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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/227,174	01/07/1999	THOMAS A. PIAZZA	42390.P6702	8615

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EXAMINER
LEE, RICHARD J

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/227,174	Piazza et al
Examiner	**Art Unit**
Richard Lee	2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 29, 2002*

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *29-50* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideratio

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *29-50* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The request filed on October 29, 2002 for a Request for Continued Examination is acceptable and a RCE has been established. An action on the RCE follows.

2. Claims 33, 43, 44, 46, 47, 49, and 50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For examples:

(1) claim 33, line 2, "the instruction" shows no clear antecedent basis;

(2) claim 43, line 2, "the instruction" shows no clear antecedent basis;

(3) claim 46, line 4, "the bounding the bounding" should be changed to "the bounding" for clarity; and

(4) claim 49, line 5, "the bounding the bounding" should be changed to "the bounding" for clarity.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 29, 31, 32, 41, 42, 45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eto et al of record (5,652,823) in view of Fujinami of record (5,337,086) and Hocevar et al (6,002,438).

Eto et al discloses a video data encoder and decoder as shown in Figures 1, 2, 7, and 15, and the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as claimed in claims 29, 31, 41, 42, 45, and 48 comprising substantially the same command stream controller (i.e., 17 of Figure 7 and see column 24, lines 14-36) to manipulate motion compensated video data; a write address generator coupled to the command stream controller (see column 35, lines 13-30); a memory (i.e., 16 of Figure 7) coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator and based on an output from an Inverse Discrete Cosine Transform operation (see Figure 2, 12 of Figure 7, Figure 15I, column 4, column 24, lines 5-13, and column 35, lines 13-30); processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame (see Figures 2 and 7); a read address generator (see column 35, lines 13-30) coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output the pixel data in a second order (see Figure 15J, column 4, and column 35, lines 13-30); wherein the first order corresponds to an output sequence of an inverse discrete cosine transform operation (see Figure 2 and column 24, lines 5-13); receiving a motion compensation command (i.e., decoding control circuit 25 of Figure 7, see

column 24, lines 5-67) having associated correction data related to a macroblock; storing the correction data in a memory (i.e., 16 of Figure 7 and see Figure 15I, column 4, column 35, lines 13-30) block by block according to a first order; performing frame prediction operations (see Figure 2) in response to the motion compensation command; reading the correction data from the memory (see Figure 15J, column 4, and column 35, lines 13-30); combining the correction data with results from the frame prediction operations to generate an output video frame (i.e., as provided by 413 of Figure 2, see column 4, column 24, lines 5-67);.

Eto et al does not particularly disclose, though, the followings:

(a) wherein the second order comprises reading the pixel data sub-block-by-sub-block row major order as claimed in claims 29 and 41; and

(b) wherein the first order is block by block in row major order, storing the correction data in a memory block by block in row major order, and reading the correction data from the memory sub-block by sub-block in row major order as claimed in claims 32, 42, 45, and 48.

Regarding (a) and (b), Fujinami discloses an image signal coding and decoding apparatus with multiple process motion compensation as shown in Figures 1, 3-6, and teaches the conventional breakdown of macroblocks into subblocks and the use of a read address generator for the selection of macroblock or subblock motion compensation processings (see column 4, lines 39-52, columns 7-9, Figures 1 and 6). It is noted that Fujinami is silent as to whether the blocks and subblocks stored and retrieve from memory are based on the row major orders as claimed. However, Hocevar et al discloses a method and apparatus for storing decoded video

information as shown in Figures 1 and 2, and teaches the conventional storage and retrieval of blocks in a row major order fashion (see column 7, lines 9-48). It is hence considered obvious to provide the row major order storage and retrieval of blocks as taught by Hocevar et al as the specific method for the processing of data within the memory system of Fujinami. Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto et al, Fujinami, and Hocevar et al references in front of him/her and the general knowledge of block processings within motion compensation video systems, would have had no difficulty in providing a first order being block by block in row major order, storing the correction data in a memory block by block in row major order, reading the correction data from the memory sub-block by sub-block in row major order, and reading the pixel data in subblock by subblock major order as part of the reading and writing of block and subblock data within Eto et al in view of the teachings of the combination of Fujinami and Hocevar et al for the same well known selective block processings as claimed.

5. Claims 33, 34, 43, 44, 46, 47, 49, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Eto, Fujinami, and Hocevar et al as applied to claims 29, 31, 32, 41, 42, 45, and 48 in the above paragraph (4), and further in view of Mizobata et al of record (5,892,518).

The combination of Eto, Fujinami, and Hocevar et al discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated

video, and article of manufacture as above, but does not particularly disclose the followings:

(a) wherein performing frame prediction operations comprises generating a bounding box containing the macroblock, iterating the bounding box, fetching reference pixels, filtering the reference pixels, averaging the filtered reference pixels, if necessary, and adding correction data to the reference pixels as claimed in claims 46 and 49;

(b) performing texturing operations for the macroblock as claimed in claims 47 and 50; and

(c) the processing circuitry comprises a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding box are processed as claimed in claims 33, 34, 43 and 44.

Regarding (a) to (c), Mizobata et al discloses an image generating apparatus with pixel calculation circuit including texture mapping and motion compensation as shown in Figures 1, 2, 4A, 4B, 9, 10-12, 14A, 14B, 16, 17, 19A, 19B, 21, 22, 40, 41, and 43, and teaches substantially the same frame prediction operations comprising means for generating a bounding box, means for iterating the bounding box, means for fetching reference pixels, means for filtering the reference pixels, means for averaging the filtered reference pixels, if necessary, and means for adding correction data to the reference pixels (see 3009, 3010 of Figure 40, Figures 9-12, and 41-43); means for performing texturing operations for the macroblock (see Figures 10-12, and columns

28-30); and processing circuitry comprising a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding box are processed (see Figures 9-12, 40-43). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, and Mizobata et al references in front of him/her and the general knowledge of motion compensation and texture image processings, would have had no difficulty in providing the bounding box of macroblock data including the manipulation of pixels thereby containing all edges of a macroblock as well as texture operations as taught by Mizobata et al for the video imaging system of Eto for the same well known purposes as claimed.

6. Claims 30 and 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Eto, Fujinami, and Hocevar et al as applied to claims 29, 31, 32, 41, 42, 45, and 48 in the above paragraph (4), and further in view of Herrera of record (6,208,350).

The combination of Eto, Fujinami, and Hocevar et al discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as above, further including a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations (see Figures 2 and 7); memory to store reference pixels (see 407, 408 of Figure 2); mapping address generator to provide read addresses for the reference pixels (see

column 35, lines 13-30); a first in first out buffer (see Figure 8); the read address generator coupled to a write address generator, the write address generator to generate synch points and the read address generator to receive the synch points to prevent the read address generator from overwriting valid data in the memory (see column 24, lines 46-62, column 35, lines 13-30).

The combination of Eto, Fujinami, and Hocevar et al does not particularly disclose, though, the processing unit/processing circuitry to perform texture mapping operations utilizing common circuitry; a bilinear filter coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels; the first in first out buffer coupling the mapping address generator to the bilinear filter, the buffer to maintain sequence of the read addresses from the mapping address generator to the bilinear filter as claimed in claims 30, 36, and 38. However, Herrera discloses a method and apparatus for processing DVD video as shown in Figures 1 and 7, and teaches the conventional texture mapping operations and bilinear filterings within motion compensation systems (see column 14, lines 45-60). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, and Herrera references in front of him/her and the general knowledge of motion compensation video systems, would have had no difficulty in providing the texture mapping operations and bilinear filterings of Herrera within the motion compensated video system of Eto for further providing substantially the same if not the same texture mapping operations utilizing common circuitry, the bilinear filtering coupled to the memory, the bilinear filter to access the reference pixels from the memory and to

filter the reference pixels, and the first in first out buffer coupling the mapping address generator to the bilinear filter purposes as claimed.

7. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Eto, Fujinami, and Hocevar et as applied to claims 29, 31, 32, 41, 42, 45, and 48 in the above paragraph (4), and further in view of Tourtier et al of record (5,446,495).

The combination of Eto, Fujinami, and Hocevar et al discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as above, but does not particularly disclose wherein the circuit is pipelined as claimed in claim 35. However, the particular motion compensation pipeline processings are old and well recognized in the art, as exemplified by Tourtier et al (see Figures 5 and 7). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, and Tourtier et al references in front of him/her and the general knowledge of pipeline processings within motion compensation video systems, would have had no difficulty in providing the multiple frame prediction operations in response to multiple motion compensation commands in a pipeline manner as taught by Tourtier et al as part of the motion compensation video system of Eto for the same well known purposes as claimed.

8. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eto, Fujinami, Hocevar et al, and Herrera as applied to claims 29-32, 36-39, 41, 42, 45, and 48 in the above paragraphs (4) and (6), and further in view of Tourtier et al of record (5,446,495).

The combination of Eto, Fujinami, Hocevar et al, and Herrera discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as above, but does not particularly disclose the apparatus is pipelined as claimed in claim 40. However, the particular motion compensation pipeline processings and multiple frame prediction operations are old and well recognized in the art, as exemplified by Tourtier et al (see Figures 5 and 7). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, Herrera, and Tourtier et al references in front of him/her and the general knowledge of pipeline processings within motion compensation video systems, would have had no difficulty in providing the multiple frame prediction operations in response to multiple motion compensation commands in a pipeline manner as taught by Tourtier et al as part of the motion compensation video system of Eto for the same well known purposes as claimed.

9. Due to the above new grounds of rejections, the Examiner wants to point out that only pertinent arguments from the amendment filed October 29, 2002 will now be addressed.

Regarding the applicants' arguments at pages 9-10 of the amendment filed October 29, 2002 concerning in general that "... The Office action argues that the cited passages teach "a write address generator" and "a read address generator". The Applicants respectfully disagree. The

cited passage merely discloses using a write/read control signal to cause frames of video data to be outputted from a switch to a memory. Neither a "write address generator" nor a "read address generator" is discussed at all ...", the Examiner wants to initially point out that: One of ordinary skill in the art is presumed to possess a certain amount of background knowledge independent of the references. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985); In re Jacoby, 309 F.2d 513, 135 USPQ 317 (C.C.P.A. 1962). The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (C.C.P.A. 1969). As shown in column 35, lines 13-30 of Eto, the storage and reading of data to/from memory 16 is in response to the write and read control signals from system controller 17. If the writing and reading of data within memory 16 are not being addressed, then how else would the data be written or read in response to the read and write control signals of Eto. It is submitted that read and write address generators, even without specific disclosure, must obviously if not inherently be part of the memory system of Eto in order to properly read and write the data intended.

Regarding the applicants' arguments at pages 13-14 of the amendment filed October 29, 2002 concerning in general that Herrera in contrast discloses a combination of a modified graphics accelerator with software to create a cost effective hybrid solution to providing a personal computer with DVD capabilities and that Herrera teaches away from Eto, the Examiner respectfully disagrees. It is submitted again that both Herrera and Eto involve the particular

encoding and decoding of video data, and that such texture mapping operations and bilinear filterings of Herrera may certainly be provided within the motion compensated video system of Eto for further providing substantially the same if not the same texture mapping operations utilizing common circuitry, the bilinear filtering coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels, and the first in first out buffer coupling the mapping address generator to the bilinear filter purposes as claimed.

10. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry)

(for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Lee whose telephone number is (703) 308-6612. The Examiner can normally be reached on Monday to Friday from 8:00 a.m. to 5:30 p.m, with alternate Fridays off.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group customer service whose telephone number is (703) 306-0377.

RICHARD LEE
PRIMARY EXAMINER

Richard Lee/rl

12/27/02